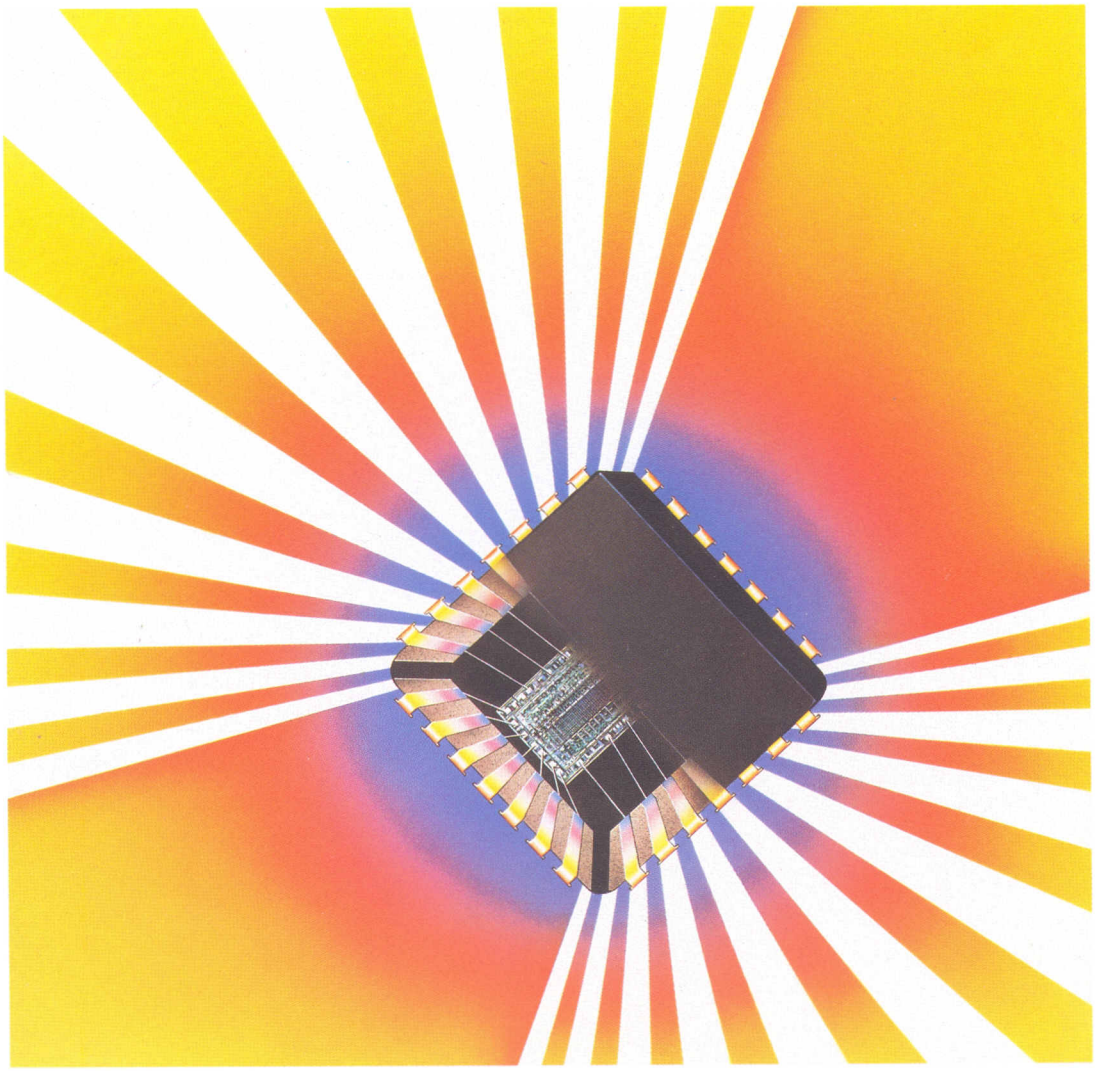
ZPAL™ Devices

1992 Data Book/Designer's Guide

Advanced
Micro
Devices



ZPAL™ Devices

1992 Data Book and Design Guide

ADVANCED MICRO DEVICES

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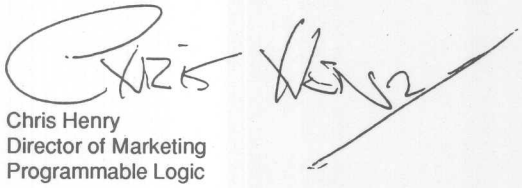
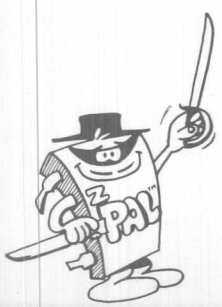
With the emergence of low-power and battery-operated equipment, it has become clear that Zero-Power Programmable Logic Devices are becoming necessary components for the future. ZPAL devices provide zero-standby power and high speed for a variety of applications.

This ZPAL Device Databook and Design Guide, consisting of datasheets and an application note, will be a valuable tool for implementing Zero-Power PLDs into your systems. With a little extra attention given to implementing a particular design, significant system power savings can be achieved.

Thanks for selecting AMD. Remember, our partnership helps you gain and keep the competitive edge. We're not your competition.



Chris Henry
Director of Marketing
Programmable Logic



ZPAL™ Devices

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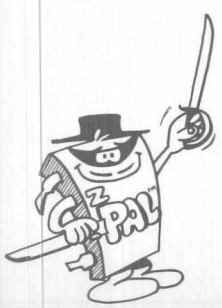


ZPAL™ Devices

COM'L: –25 IND: –25

PALCE16V8Z-25

Zero-Power 20-Pin EE CMOS Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero-Power CMOS technology**
  - 15 µA Standby Current
  - 25 ns propagation delay
- **Unused product term disable for reduced power consumption**
- **Available in industrial operating range**
  - T_C = –40°C to +85°C
  - V_{CC} = +4.5 V to +5.5 V
- **HC- and HCT-Compatible inputs and outputs**
- **Pin, function and fuse-map compatible with all 20-pin GAL® devices**
- **Electrically-erasable CMOS technology provides reconfigurable logic and full testability**
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP and PLCC packages**
- **Extensive third-party software and programmer support through FusionPLD℠ partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

The PALCE16V8Z is an advanced PAL® device built with zero-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8Z will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

The PALCE16V8Z provides zero standby power and high speed. At 15 µA maximum standby current, the PALCE16V8Z allows battery powered operation for an extended period.

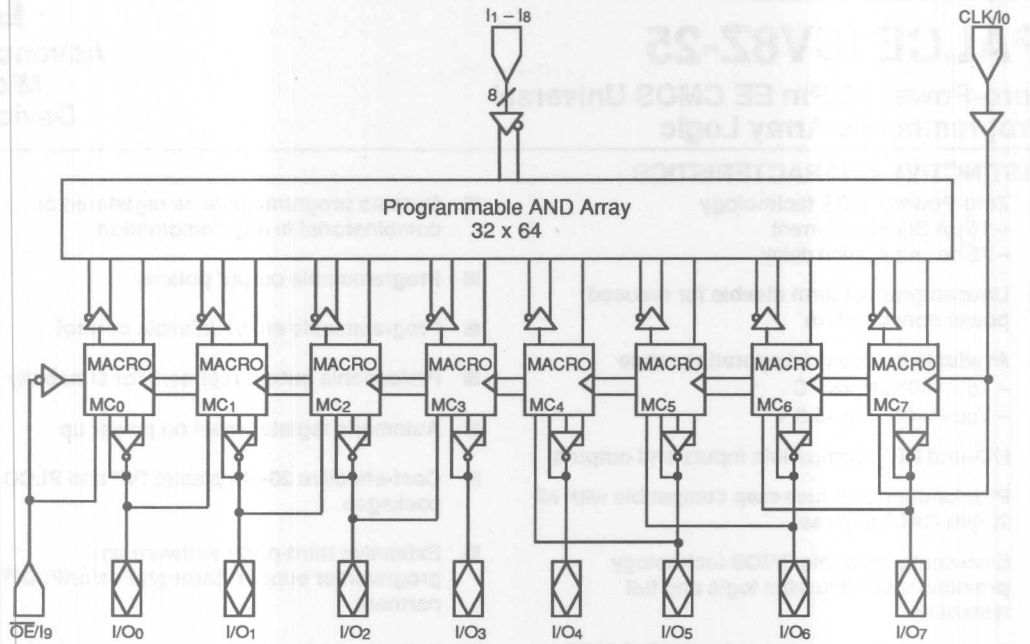
The PALCE16V8Z utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active- high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE16V8Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to page 18 or the Software Reference Guide to PLD Compilers for certified development systems, and page 20 for the Programmer Reference Guide for approved programmers.

Publication # 13061 Rev. B Amendment/0
Issue Date: June 1992

BLOCK DIAGRAM



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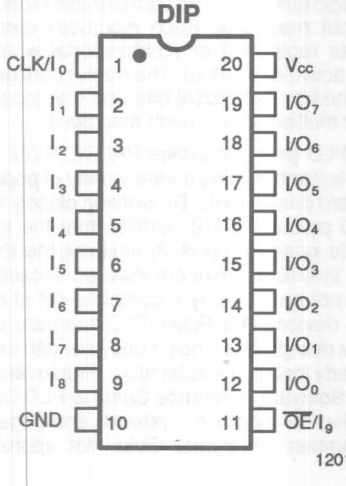
CONNECTION DIAGRAMS
Top View

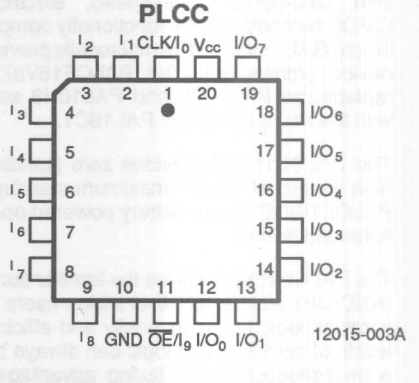
DIP



12015-002A

Note: Pin 1 is marked for orientation

PLCC



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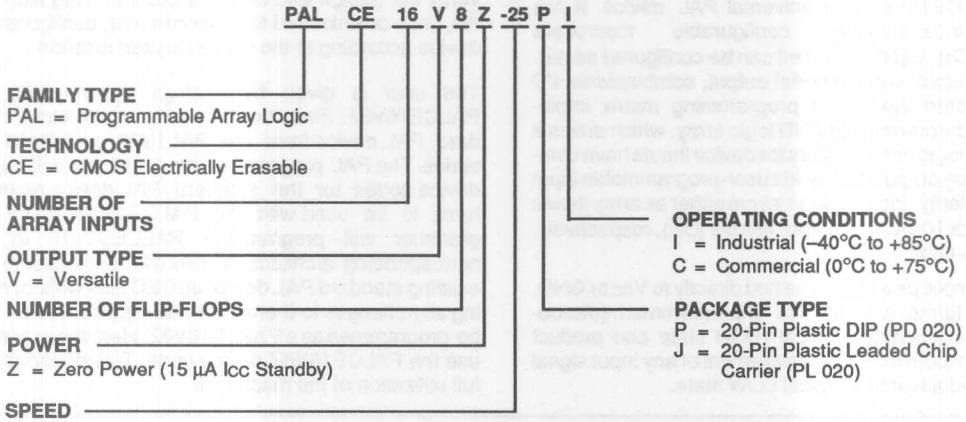
PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE16V8Z-25	PI, JI, PC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

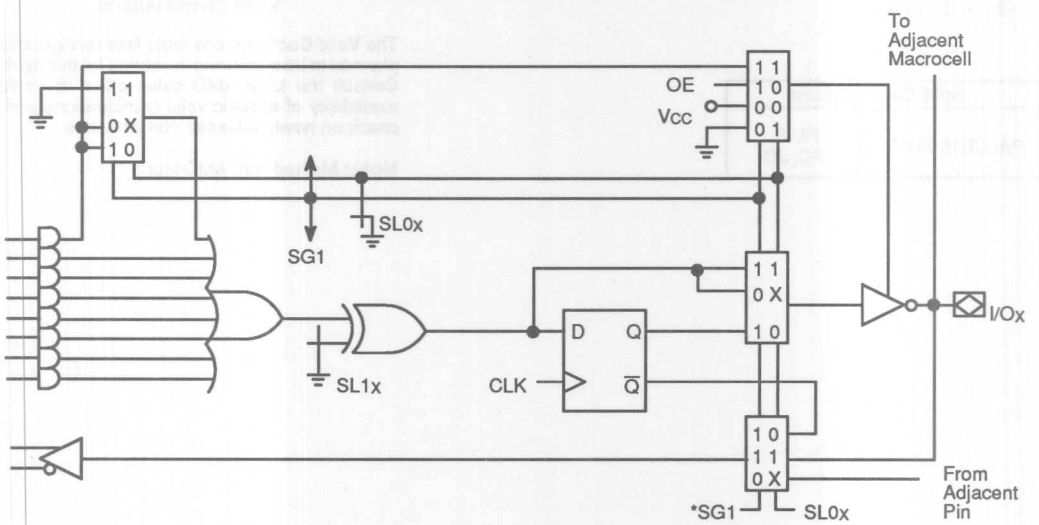
The PALCE16V8Z is the zero-power version of the PALCE16V8. It has all the architectural features of the PALCE16V8. In addition, the PALCE16V8Z has zero standby power and unused product term disable.

The PALCE16V8Z is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8Z are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8Z. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8Z. The programmer will program the PALCE16V8Z in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8Z. Here the user must use the PALCE16V8Z device code. This option allows full utilization of the macrocell.



*In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

12197-004A

Figure 1. PALCE16V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8Z will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of MC_3 and MC_4. MC_3 and MC_4 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

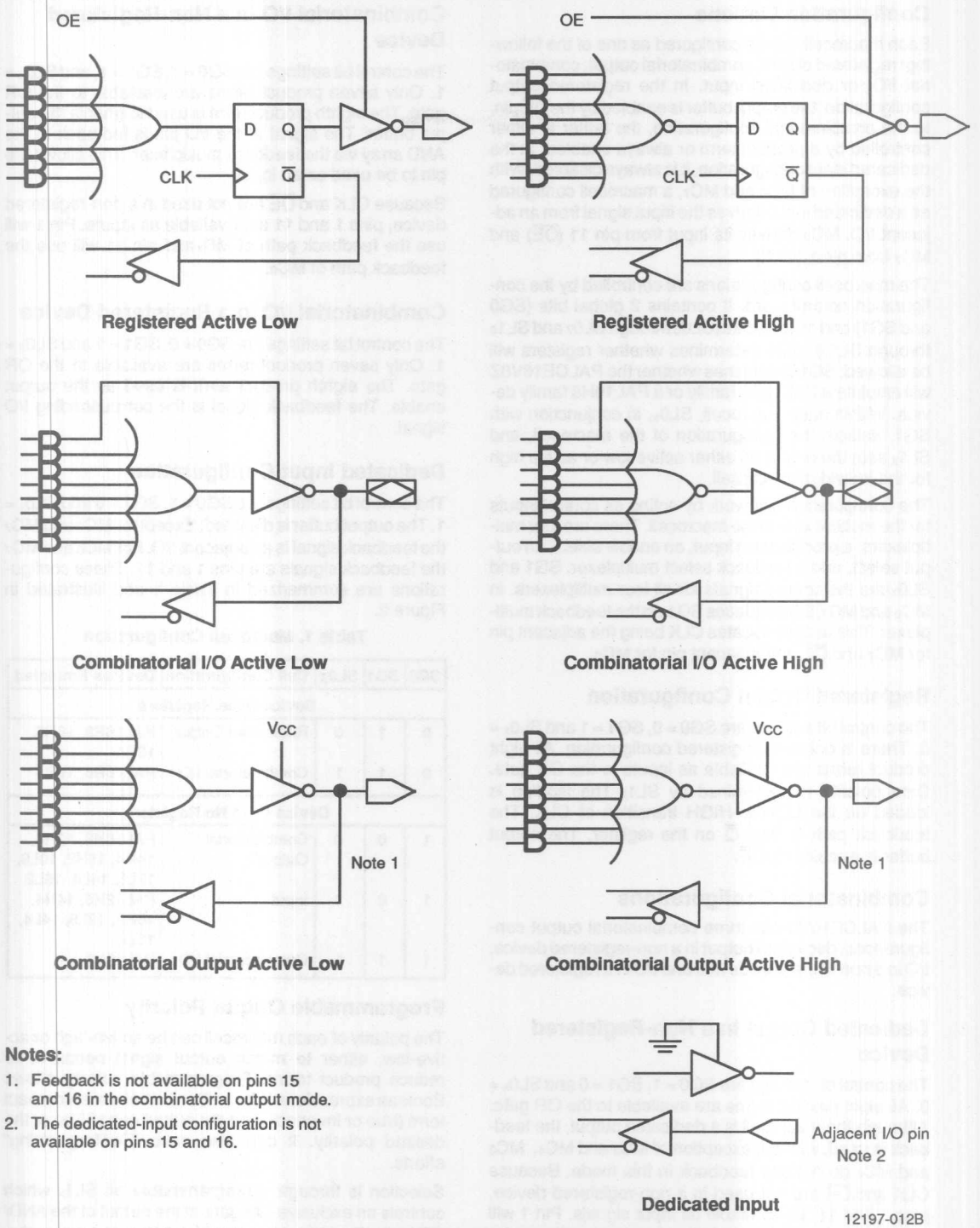
Table 1. Macrocell Configuration

SG0	SG1	$SL0_x$	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



Notes:

1. Feedback is not available on pins 15 and 16 in the combinatorial output mode.
2. The dedicated-input configuration is not available on pins 15 and 16.

Figure 2. Macrocell Configurations

Zero-Standby Power Mode

The PALCE16V8Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE16V8Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero (I_{CC} < 15 µA). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the I_{CC} vs. frequency graph on page 15.

Product-Term Disable

On a programmed PALCE16V8Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs frequency graph on page 15, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note on page 45.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8Z will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic. Details on power-up reset can be found on page 17.

Register Preload

The register on the PALCE16V8Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function is not disabled by the security bit. This allows functional testing after the security bit is programmed.

Security Bit

A security bit is provided on the PALCE16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required. Approved programmers are listed on page 20.

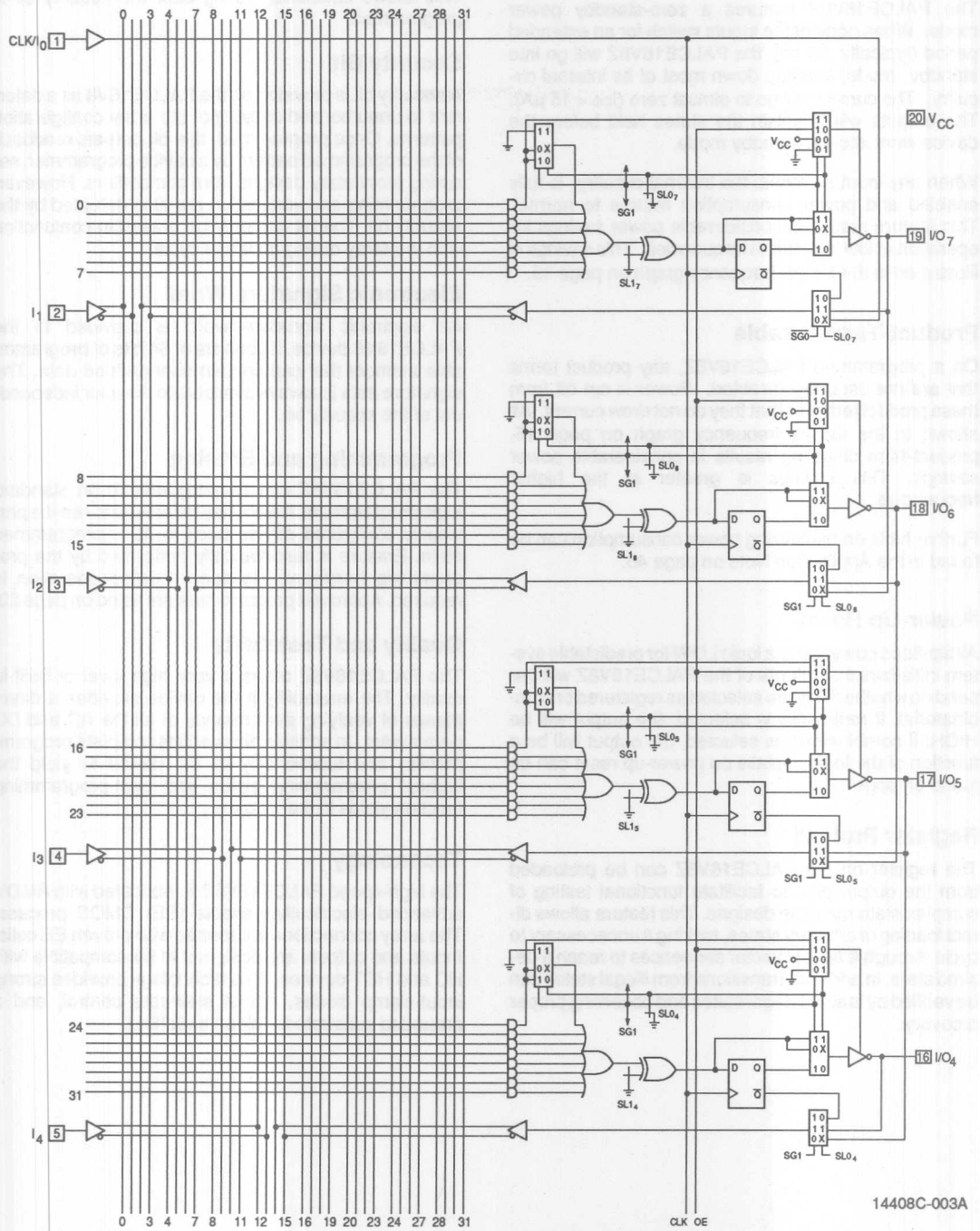
Quality and Testability

The PALCE16V8Z offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

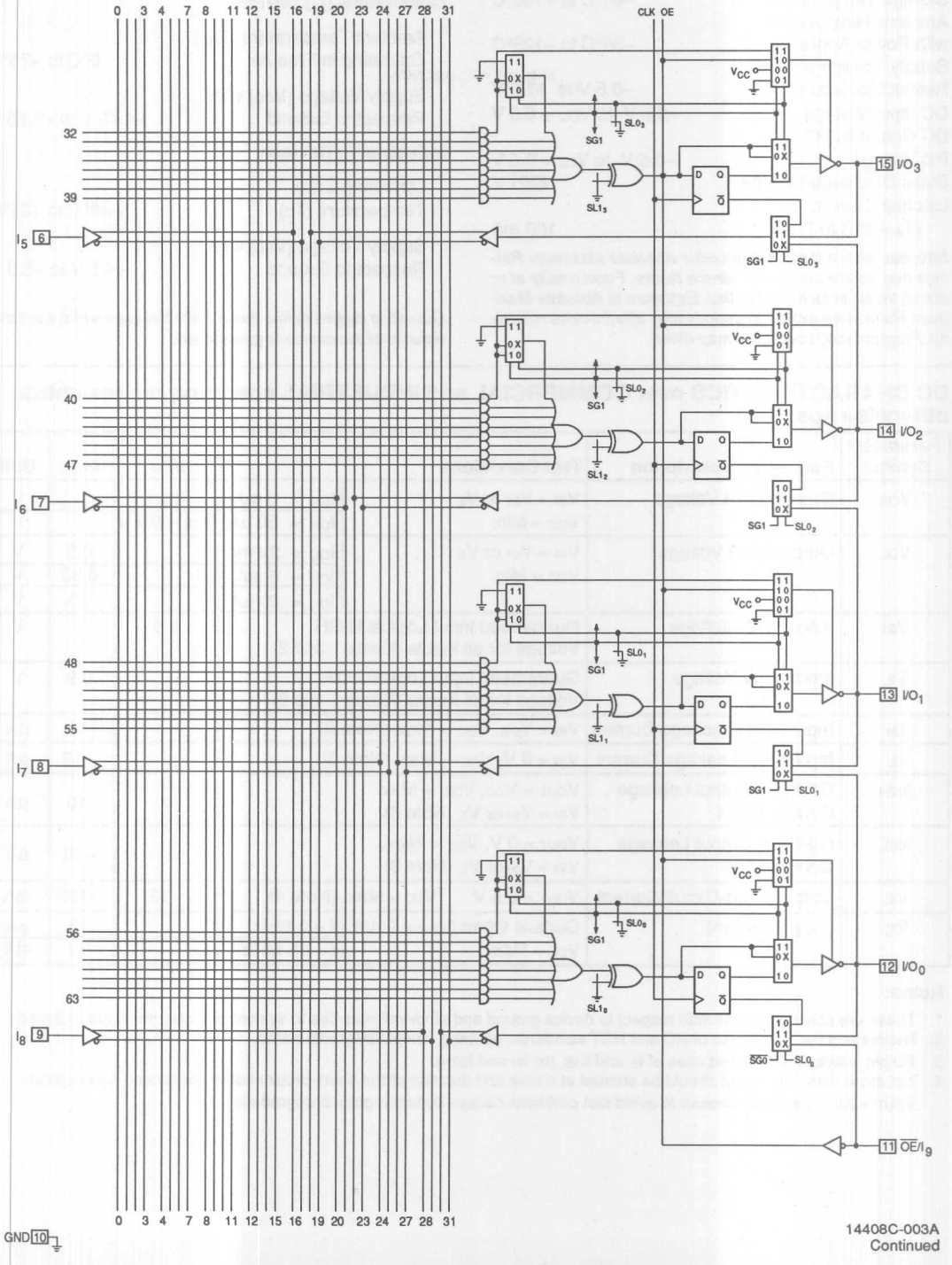
Technology

The high-speed PALCE16V8Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



LOGIC DIAGRAM (Continued)



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Continued

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Industrial (I) Devices

Operating Case Temperature (T_C)	–40°C to +85°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max. (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max. (Note 4)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.	f = 0 MHz		15	µA
			f = 25 MHz		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Represents the worst case of HC and HCT standards, allowing compatibility with either.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

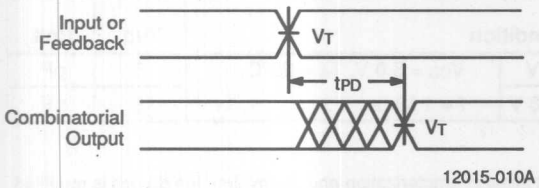
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input or Feedback to Clock			20		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(ts+tco)	33.3		MHz
		Internal Feedback (f_{CNT})		50		MHz
		No Feedback	1/(ts+tH)	50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				25	ns
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

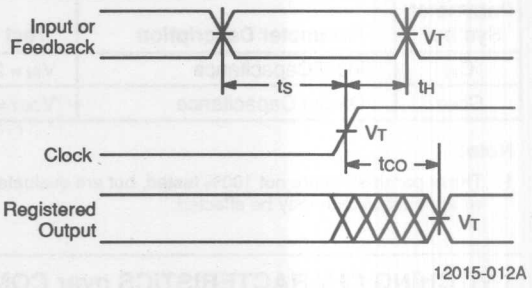
Notes:

2. See Switching Test Circuit for test conditions.
3. This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 2 ns faster.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

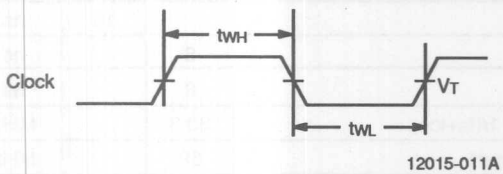
SWITCHING WAVEFORMS



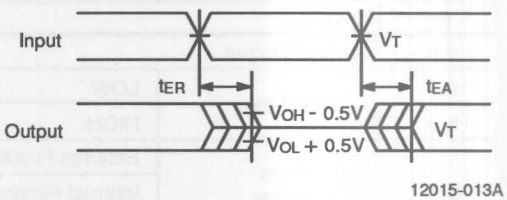
Combinatorial Output



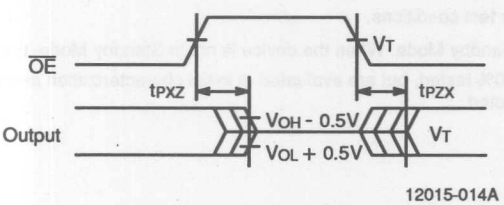
Registered Output



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

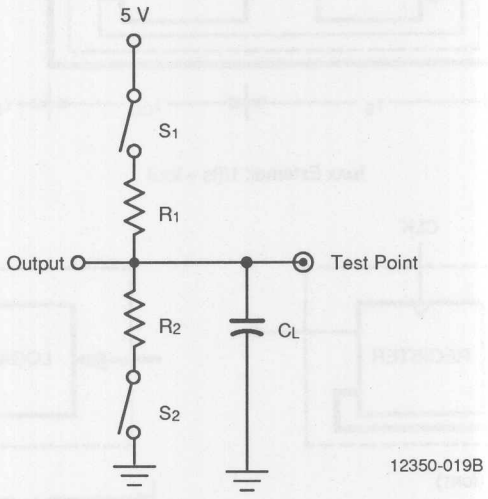
1. V_T = 1.5 V for Input Signals and 2.5 V for Output Signals.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019B

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	820 Ω	820 Ω	2.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				2.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

f_{MAX} Parameters

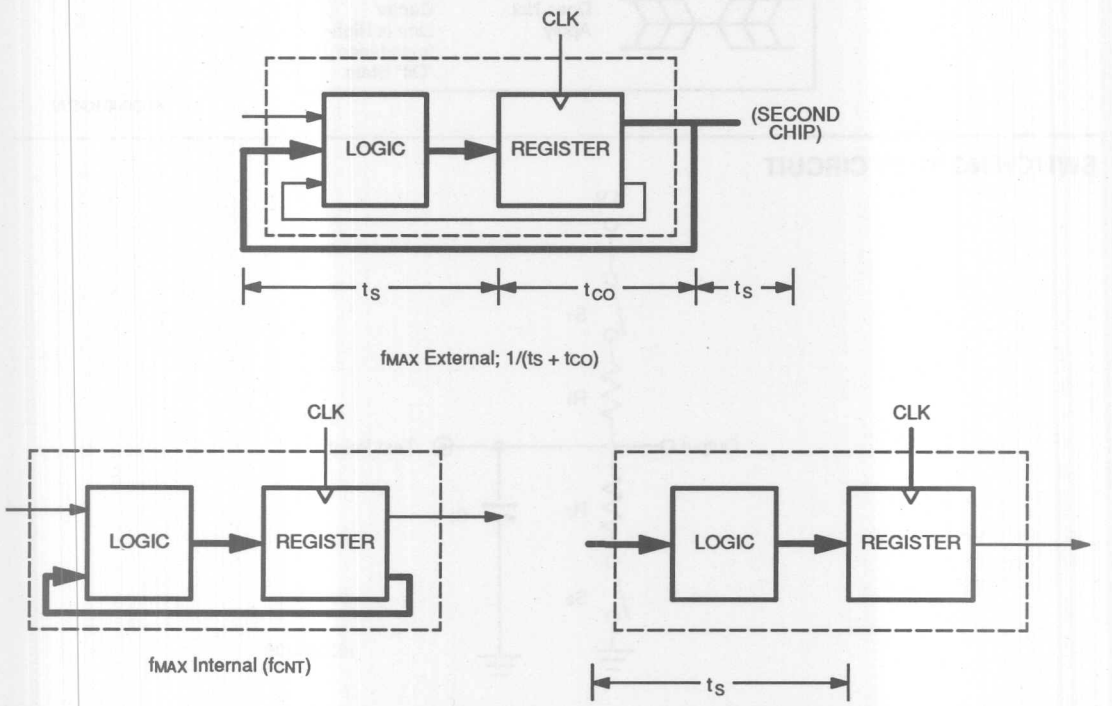
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design, therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback".

f_{MAX} external and f_{MAX} no feedback are calculated parameters. f_{MAX} external is calculated from t_S and t_{CO}, and f_{MAX} no feedback is calculated from t_{WL} and t_{WH}. f_{MAX} internal is measured.



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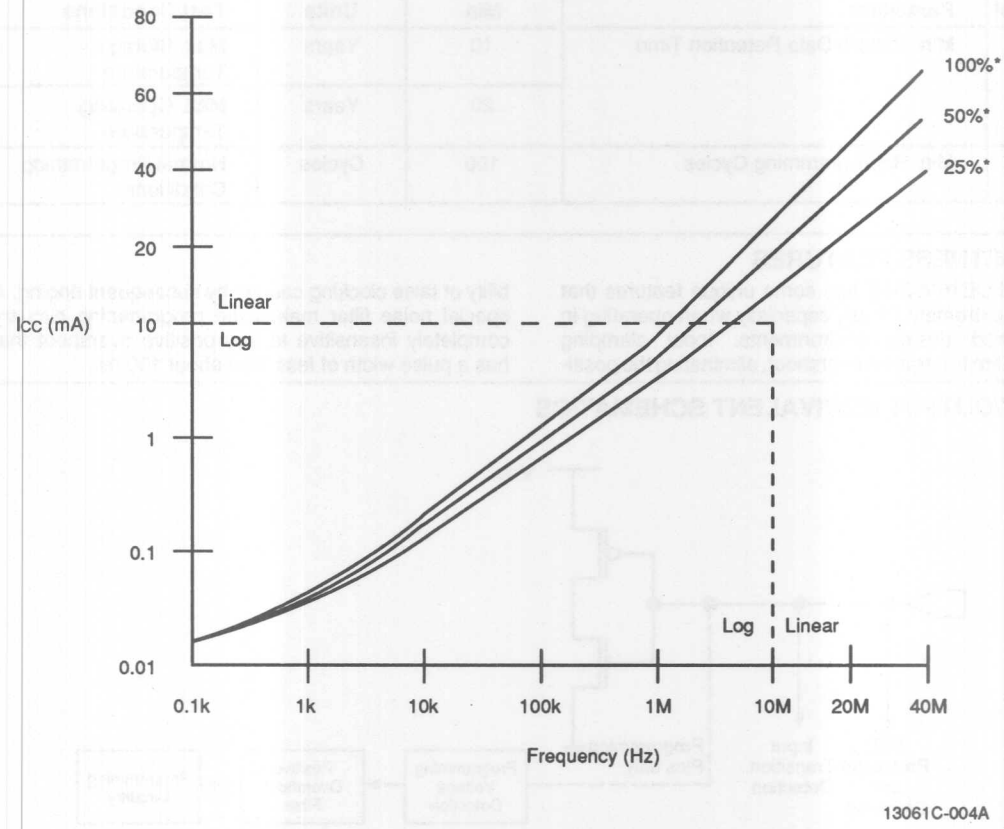
TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



*Percent of product terms used.

I_{CC} vs Frequency

ENDURANCE CHARACTERISTICS

The PALCE16V8Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

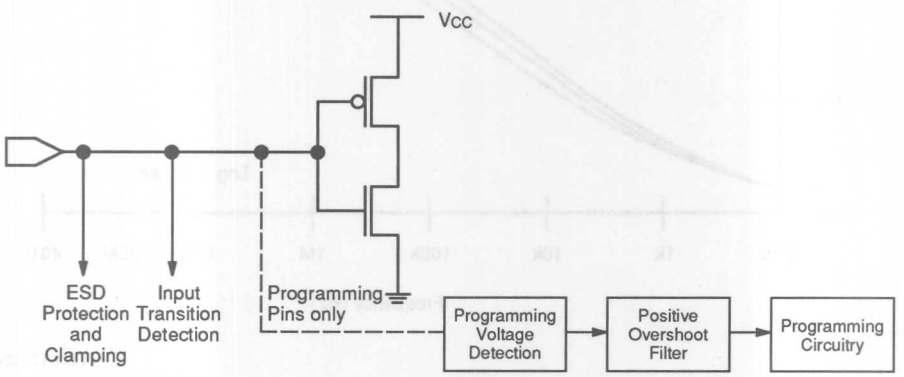
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

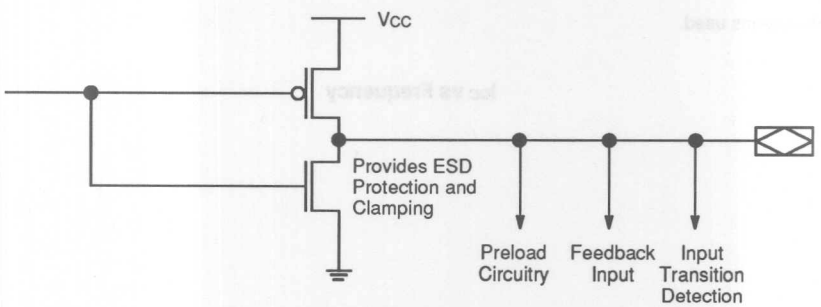
ROBUSTNESS FEATURES

The PALCE16V8Z-25 has some unique features that make it extremely robust, especially when operating in high-speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

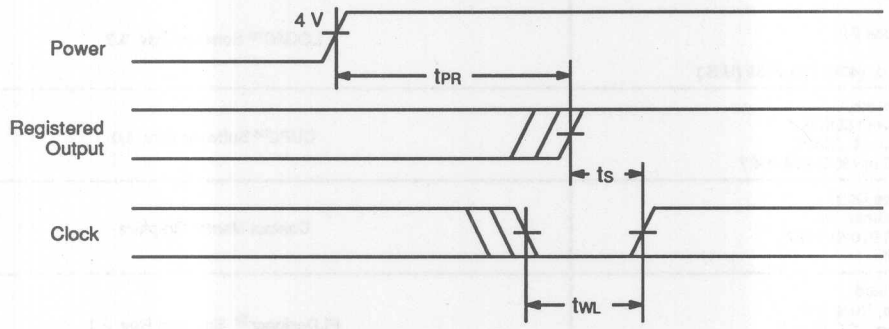
13061B-003A

POWER-UP RESET

The PALCE16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



12350-024A

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	COMPILERS
Advanced Micro Devices, Inc. 901 Thompson Place MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PALASM® Software Rev. 1.0
Cadence (Valid) Design Systems, Inc. 555 River Oaks Parkway San Jose, CA 95134 (408) 943-1234	Contact Cadence
Capilano Computing Systems, Ltd. 960 Quayside Dr., Suite 406 New Westminster, B.C. Canada V3M 6G2 (800) 444-9064 or (604) 522-6200	Contact Capilano
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™-4 Software Rev. 2.0
ISDATA GmbH Daimlerstr. 51 D-7500 Karlsruhe 21 Germany 0721/75 10 87 or (408) 373-7359 (U.S.)	LOG/iC™ Software Rev. 3.2
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software Rev. 4.0
Mentor Graphics Corp. 8005 S.W. Beckman Rd. Wilsonville, OR 97070-7777 (800) 345-2308	Contact Mentor Graphics
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PLDesigner® Software Rev. 2.1
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Programmable Logic Design Tools Rev. 4.0
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 422-4660 or (508) 480-0881	Contact Viewlogic
MANUFACTURER	**SCHEMATIC EDITORS AND LIBRARIES**
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Contact OrCAD
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 32-8246 or (206) 881-6444	Contact Data I/O

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	SIMULATORS
ALDEC Company, Inc. 3525 Old Conejo Rd., Suite 111 Newbury Park, CA 91320 (805) 499-6867	Contact ALDEC
Cadence (Valid) Design Systems, Inc. 555 River Oaks Parkway San Jose, CA 95134 (408) 943-1234	Contact Cadence
iNt GmbH Bunsenstrasse 6 D-8033 Martinsreid/Munich Germany (89) 857-6667	Contact iNt
Logic Automation Inc. 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	Contact Logic Automation
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Contact OrCAD
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 422-4660 or (508) 480-0881	Contact Viewlogic
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	Contact Acugen
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	Contact Data I/O
iNt GmbH Bunsenstrasse 6 D-8033 Martinsreid/Munich Germany (89) 857-6667	Contact iNt

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APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

Manufacturer	Programmer Configuration
Advanced Micro Devices, Inc. 901 Thompson Pl. Sunnyvale, CA 94088 (800) 222-9323 or (408) 732-2400	LabPro™ Rev. A1.3
Advin Systems, Inc. 1050-L East Duane Avenue Sunnyvale, CA 94086 (408) 243-7000	U40 Rev. 10.36 U80 Rev. 10.36
BP Microsystems 10681 Haddington, Suite #190 Houston, TX 77043 (800) 225-2102 or (713) 461-9430	PLD-1128 Rev. 1.86
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite™ DIP: Rev. 3.6 Model 2900 Rev. 1.9 M3900 Rev. 1.3 Family/Pinout Codes: 80-E1
Digelec, Inc. 20144 Plummer St. Chatsworth, CA 91311 (800) 367-8750 or (818) 701-9677 or Digitronics 25 Galgaley Haplada St. Herzliya B46722, Israel 52-55-9615	ALLPRO88 Rev. 2.2
Logical Devices, Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	Contact Logical Devices
Microprоss Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	Contact Microprоss

APPROVED PROGRAMMERS (Continued) (subject to change)

Manufacturer	Programmer Configuration
SMS North America, Inc. 16552 NE 135th Pl. Redmond, WA 98052 (800) 722-4122 or (206) 883-8447 or SMS Im Morgental 13 D-8994 Hergatz, Germany 07522-5018	Contact SMS
Stag Microsystems 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	Contact Stag
System General Corp. 510 S. Park Victoria Dr. Milpitas, CA 95035 (408) 263-6667 or System General Corp. 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	Contact System General

ZPAL™ Devices

Advanced Micro Devices

PALCE22V10Z-25

Zero-Power 24-Pin EE CMOS Versatile PAL Device

DISTINCTIVE CHARACTERISTICS

- **Zero-power CMOS technology**
  - 15 µA standby current
  - 25 ns first-access propagation delay
- **Unused product term disable for reduced power consumption**
- **Available in Industrial operating range**
  - T_C = –45°C to +85°C
  - V_{CC} = +4.5 V to +5.5 V
- **HC- and HCT-compatible inputs and outputs**
- **Electrically-erasable technology provides reconfigurable logic and full testability**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP® and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PALCE22V10Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It provides user-programmable logic for replacing conventional zero-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

The PALCE22V10Z provides zero standby power and high speed. At 15 µA maximum standby current, the PALCE22V10Z allows battery powered operation for an extended period.

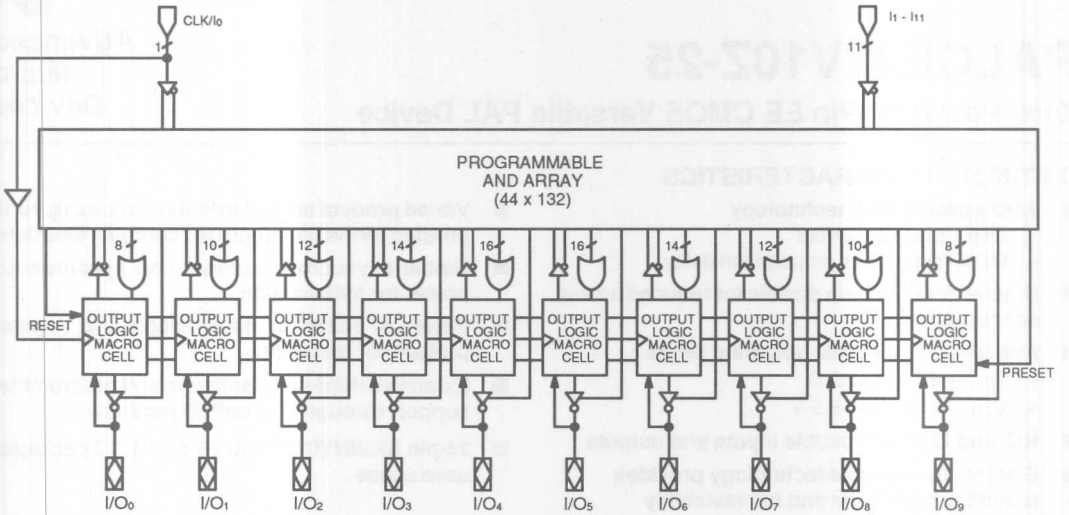
The ZPAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to page 38 or the Software Reference Guide to PLD Compliers for certified development systems, and page 40 or the Programmer Reference Guide for approved programmers.

Publication# 15700 Rev. B Amendment/0
Issue Date: June 1992

BLOCK DIAGRAM



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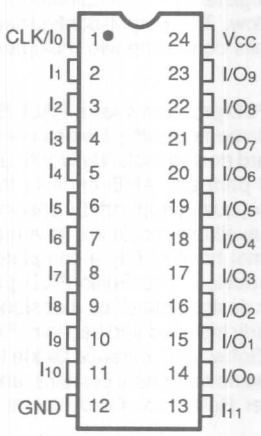
CONNECTION DIAGRAMS

Top View

SKINNYDIP



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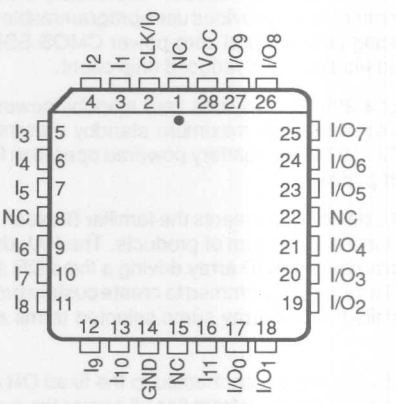
PLCC



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Note:
Pin 1 is marked for orientation.

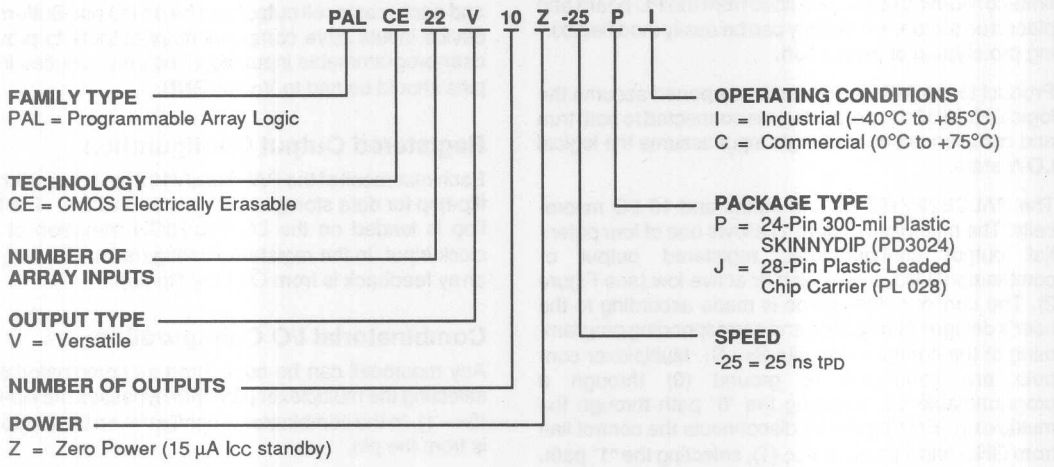
PIN DESCRIPTION

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
VCC = Supply Voltage

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
PALCE22V10Z-25	PI, JI, PC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE22V10Z is the zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALCE22V10Z has zero standby power and unused product term disable.

The PALCE22V10Z allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10Z has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

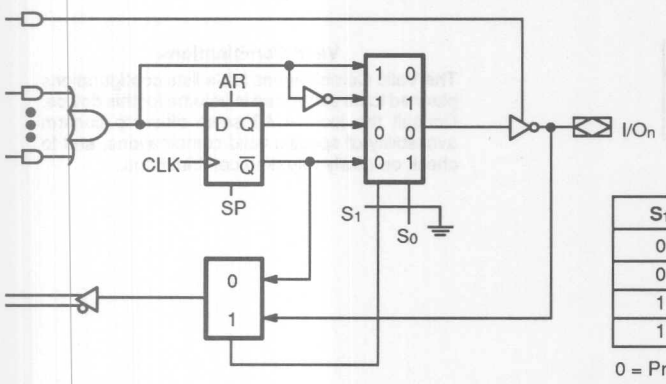
The PALCE22V10Z has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PALCE22V10Z includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

09849-004A

Figure 1. Output Logic Macrocell

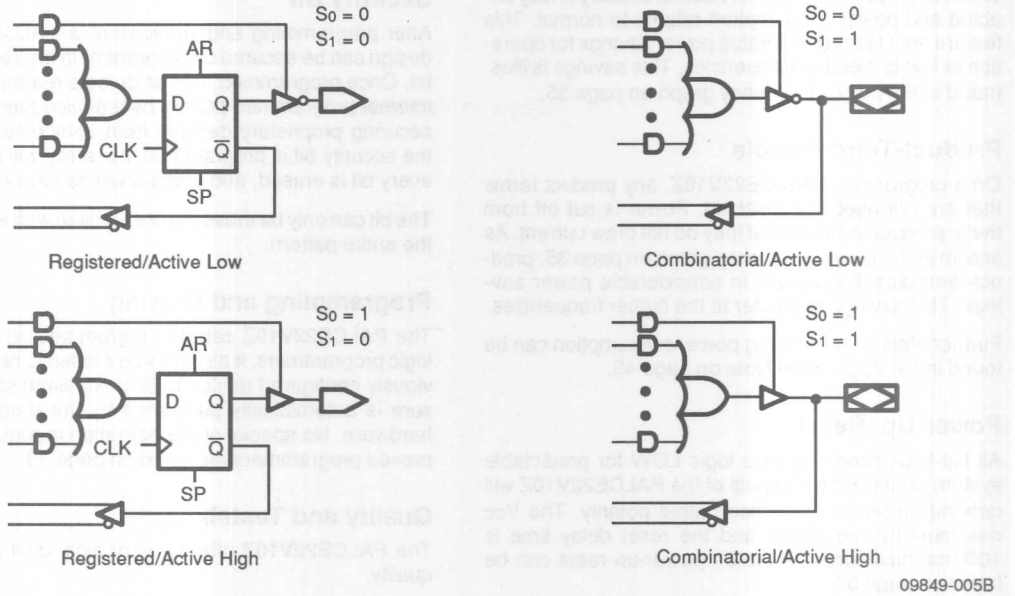


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10Z has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Zero-Standby Power Mode

The PALCE22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE22V10Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero ($I_{CC} < 15\ \mu A$). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the Icc vs. frequency graph on page 35.

Product-Term Disable

On a programmed PALCE22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the Icc vs. frequency graph on page 35, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note on page 45.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10Z will depend on the programmed output polarity. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum. Details on power-up reset can be found on page 37.

Register Preload

The registers on the PALCE22V10Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10Z design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required. Approved programmers are listed on page 40.

Quality and Testability

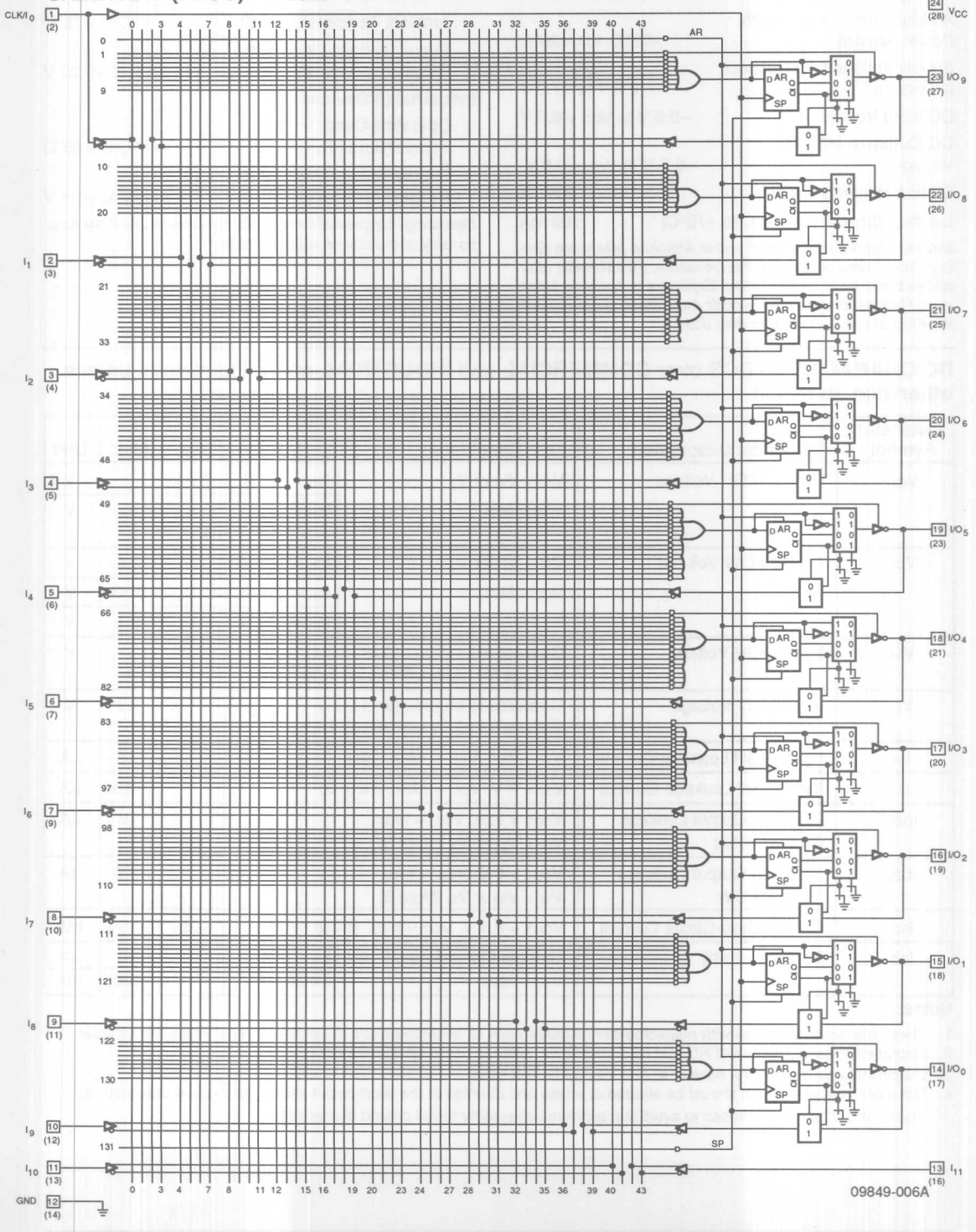
The PALCE22V10Z offers a very high level of built-in quality.

The erasability of the CMOS PALCE22V10Z allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALCE22V10Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Industrial (I) Devices

Operating Case Temperature (T_C)	–45°C to +85°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min.	I_{OH} = 20 µA	V_{CC}– 0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
		V_{CC} = Min.	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max. (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 4)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		15	µA
		V_{CC} = Max.	f = 25 MHz		120	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Represents the worst case of HC and HCT standards, allowing compatibility with either.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

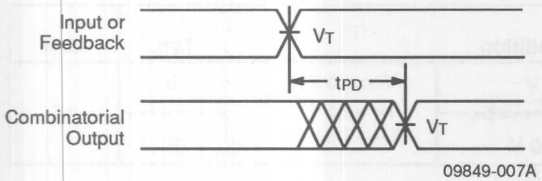
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})		35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

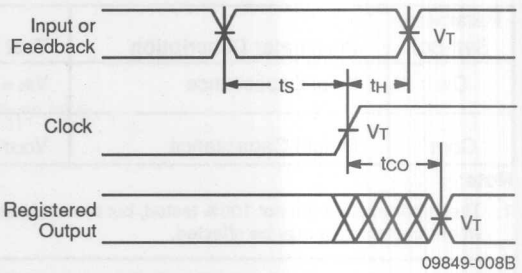
Notes:

2. See Switching Test Circuit for test conditions.
3. This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 5 ns faster.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

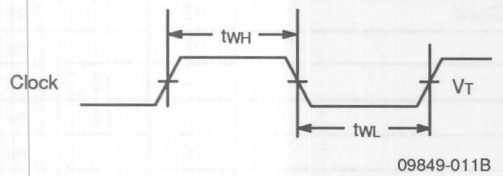
SWITCHING WAVEFORMS



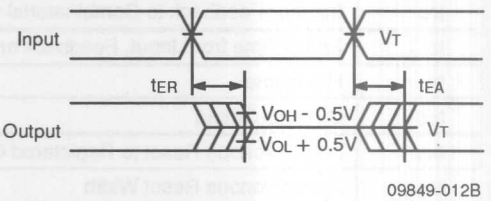
Combinatorial Output



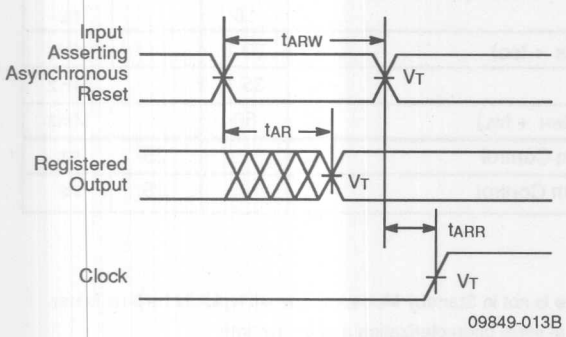
Registered Output



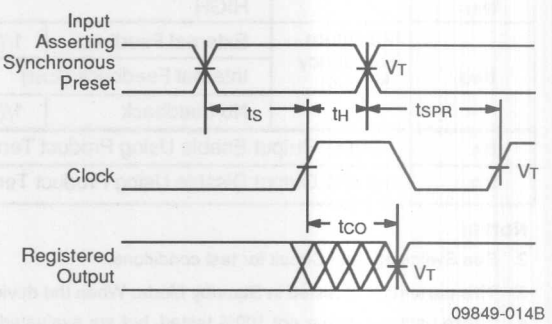
Clock Width



Input to Output Disable/Enable



Asynchronous Reset

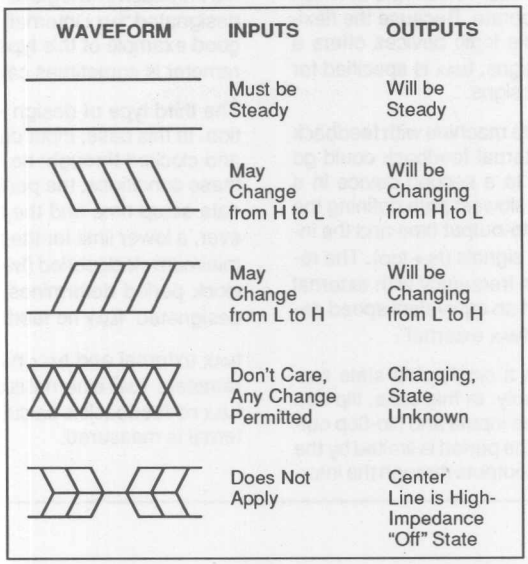


Synchronous Preset

Notes:

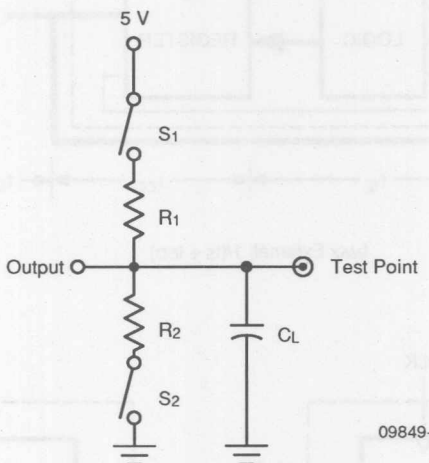
1. V_T = 1.5 V for Input Signals and 2.5 V for Output Signals.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



09849-015B

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	820 Ω	820 Ω	2.5 V
t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				2.5 V
t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

f_{MAX} Parameters

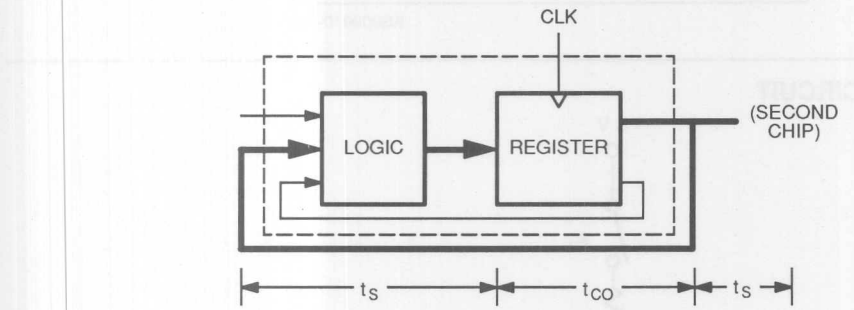
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

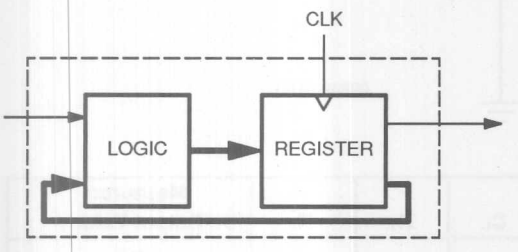
The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design, therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback".

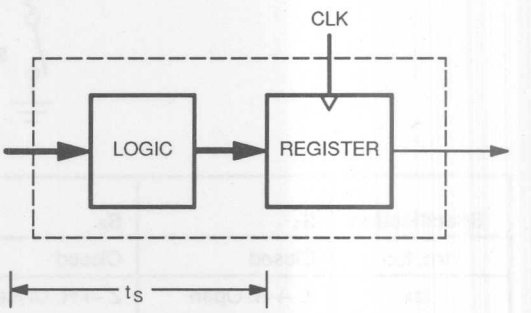
f_{MAX} external and f_{MAX} no feedback are calculated parameters. f_{MAX} external is calculated from t_S and t_{CO}, and f_{MAX} no feedback is calculated from t_{WL} and t_{WH}. f_{MAX} internal is measured.



f_{MAX} External; $1/(t_S + t_{CO})$



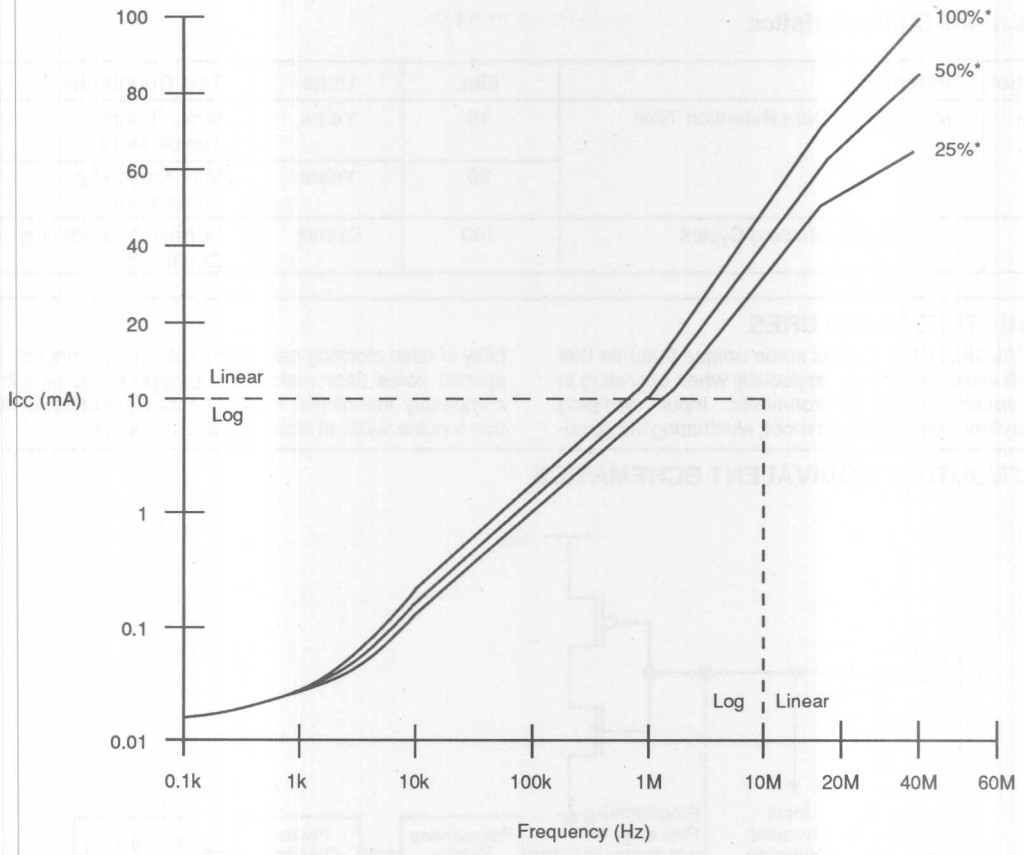
f_{MAX} Internal (f_{CNT})



f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

12222C-007B

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5.0 V, T_A = 25°C



15700A-002B

*Percent of product terms used.

I_{CC} vs. Frequency

ENDURANCE CHARACTERISTICS

The PALCE22V10Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

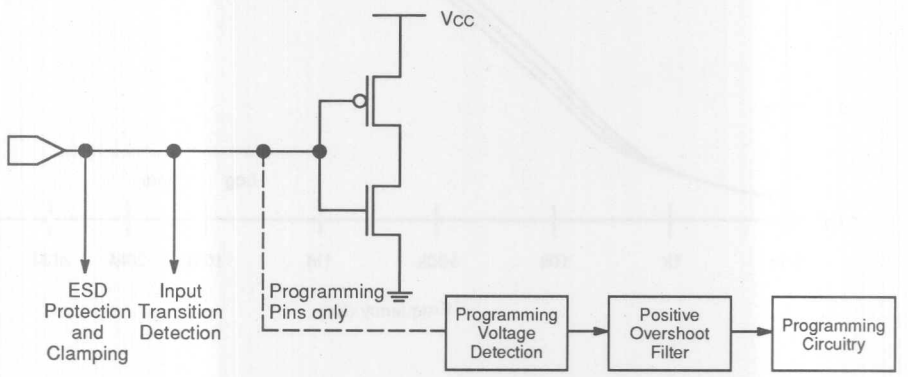
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

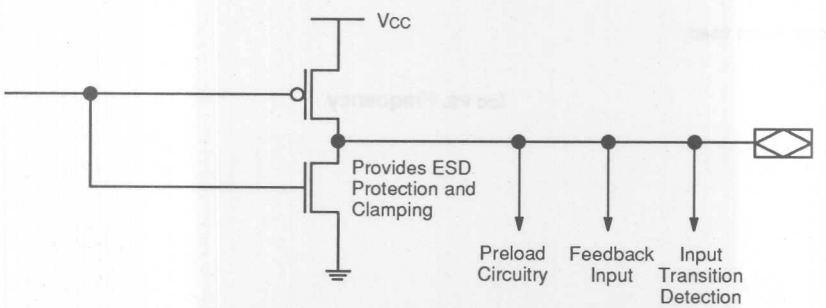
ROBUSTNESS FEATURES

The PALCE22V10Z-25 has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

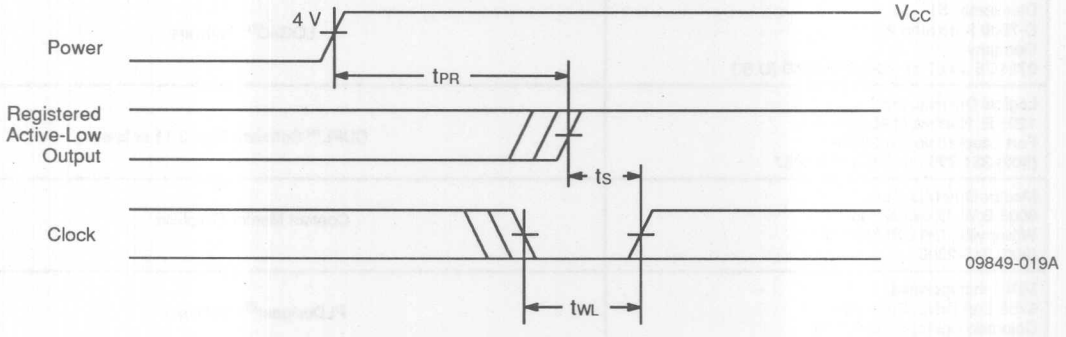
13061B-003A

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
ts	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	COMPILERS
Advanced Micro Devices, Inc. 901 Thompson Place MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PALASM® Software Rev. 2.2 or later
Cadence (Valid) Design Systems, Inc. 555 River Oaks Parkway San Jose, CA 95134 (408) 943-1234	Contact Cadence
Capilano Computing Systems, Ltd. 960 Quayside Dr., Suite 406 New Westminster, B.C. Canada V3M 6G2 (800) 444-9064 or (604) 522-6200	Contact Capilano
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™-4 Software Rev. 2.0 or later
ISDATA GmbH Daimlerstr. 51 D-7500 Karlsruhe 21 Germany 0721/75 10 87 or (408) 373-7359 (U.S.)	LOG/iC™ Software
Logical Devices, Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software Rev. 2.11 or later
Mentor Graphics Corp. 8005 S.W. Beckman Rd. Wilsonville, OR 97070-7777 (800) 345-2308	Contact Mentor Graphics
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PLDesigner® Software
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Programmable Logic Design Tools
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 422-4660 or (508) 480-0881	Contact Viewlogic
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DEVELOPMENT SYSTEMS (subject to change)

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MANUFACTURER	SIMULATORS
ALDEC Company, Inc. 3525 Old Conejo Rd., Suite 111 Newbury Park, CA 91320 (805) 499-6867	Contact ALDEC
Cadence (Valid) Design Systems, Inc. 555 River Oaks Parkway San Jose, CA 95134 (408) 943-1234	Contact Cadence
iNt GmbH Bunsenstrasse 6 D-8033 Martinsreid/Munich Germany (89) 857-6667	Contact iNt
Logic Automation Inc. 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	Contact Logic Automation
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Contact OrCAD
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 422-4660 or (508) 480-0881	Contact Viewlogic
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Software
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	PLDtest™ Plus Software
iNt GmbH Bunsenstrasse 6 D-8033 Martinsreid/Munich Germany (89) 857-6667	Contact iNt

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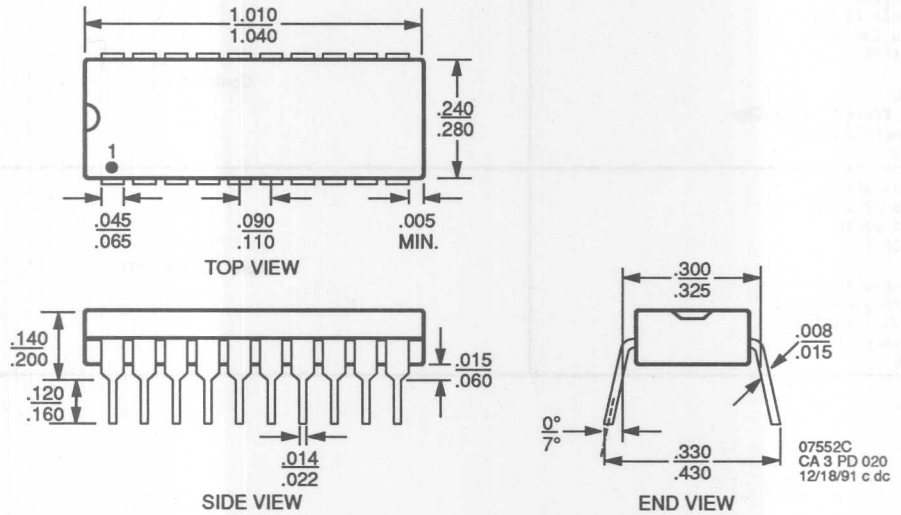
Manufacturer	Programmer Configuration
Advanced Micro Devices, Inc. 901 Thompson Pl. Sunnyvale, CA 94088 (800) 222-9323 or (408) 732-2400	LabPro™ Rev. 1.3
Advin Systems, Inc. 1050-L East Duane Avenue Sunnyvale, CA 94086 (408) 243-7000	U40 Rev. 10.36 U84 Rev. 10.36
BP Microsystems 10681 Haddington, Suite #190 Houston, TX 77043 (800) 225-2102 or (713) 461-9430	PLD-1128 Rev. 1.55
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite™ DIP: Rev. 3.4 PLCC: Rev. 3.4 Family/Pinout Codes: 80-E0
Digelec, Inc. 20144 Plummer St. Chatsworth, CA 91311 (800) 367-8750 or (818) 701-9677 or Digitronics 25 Galgaley Haplada St. Herzliya B46722, Israel 52-55-9615	Contact Digelec
Logical Devices, Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	Contact Logical Devices
Microprоss Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	Contact Microprоss

APPROVED PROGRAMMERS (Continued) (subject to change)

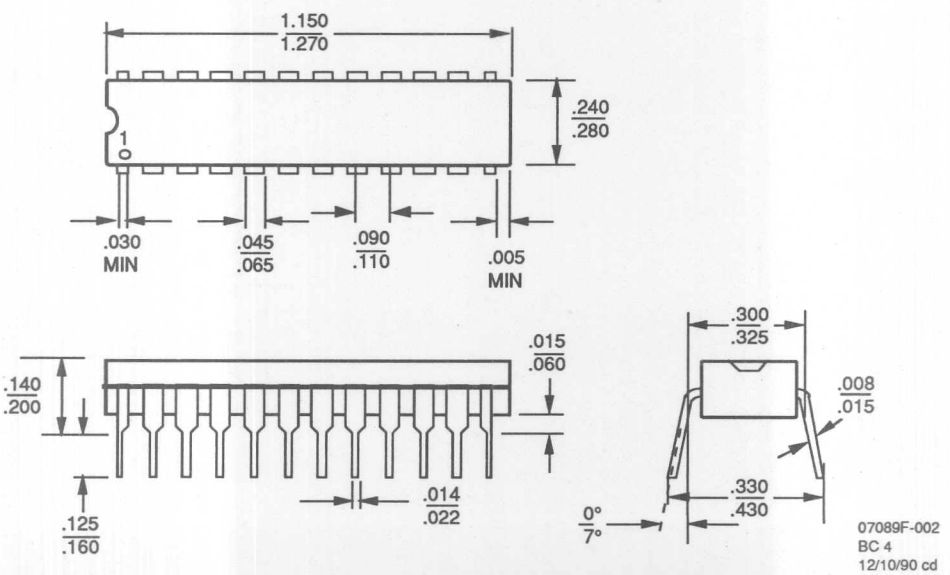
Manufacturer	Programmer Configuration
SMS North America, Inc. 16552 NE 135th Pl. Redmond, WA 98052 (800) 722-4122 or (206) 883-8447 or SMS Im Morgental 13 D-8994 Hergatz, Germany 07522-5018	Contact SMS
Stag Microsystems 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	Contact Stag
System General Corp. 510 S. Park Victoria Dr. Milpitas, CA 95035 (408) 263-6667 or System General Corp. 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	Turpro–1 Rev. 1.50

Physical Dimensions*

PD 020
20-Pin Plastic DIP

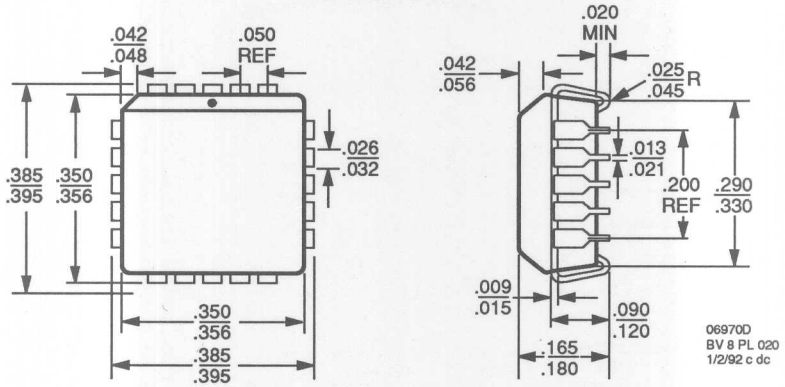


PD3024
24-Pin 300-mil Plastic SKINNYDIP

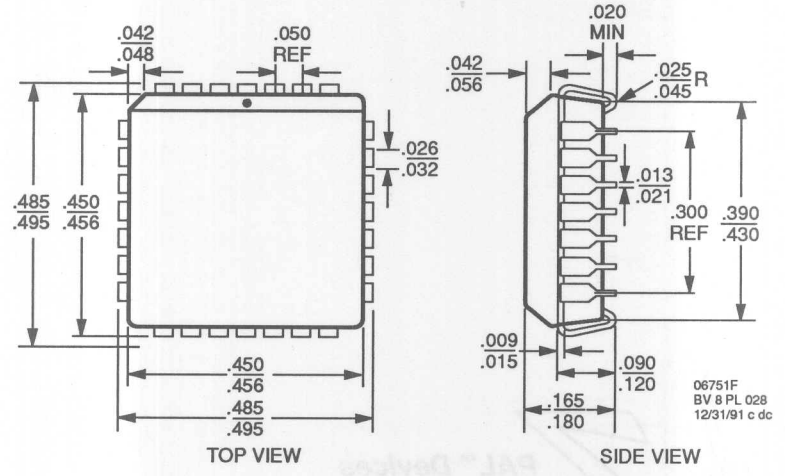


*For reference only. All dimensions measured in inches. BSC is an ANSI standard for basic space centering.

PL 020
20-Pin Plastic Leaded Chip Carrier



PL 028
28-Pin Plastic Leaded Chip Carrier



ZPAL™ Devices

Minimizing Power Consumption with Zero-Power PLDs

Application Note

by Shawn D. Worsell, Senior Applications Engineer

Advanced Micro Devices

Zero-Power Programmable Logic Devices (PLDs) are advanced PAL devices designed with ultra low-power, high-speed, electrically-erasable CMOS technology. ZPAL devices provide zero-standby power and high speed for a variety of applications. At 15 µA maximum standby current, Zero-Power devices allow battery powered operation for an extended period of time. Zero-Power CMOS devices can significantly reduce system power consumption by replacing equivalent CMOS and TTL devices.

ZPAL devices are available in the following configurations: the industry-standard 20-pin PALCE16V8Z-25 and the AMD-patented 24-pin PALCE22V10Z-25.

The PALCE16V8Z-25 is functionally compatible with all CMOS half- and quarter-power PALCE16V8 devices and will directly replace the bipolar PAL16R8 and PAL10H8 series devices with the exception of the PAL16C1.

The PALCE22V10Z-25 is functionally compatible with all 24-pin 22V10 devices, and it provides user-programmable logic for replacing conventional low-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

POTENTIAL APPLICATIONS

ZPAL devices may be used in any application where a standard 22V10 or 16V8 device would be used. Designs that are currently in a 20V8 will also fit in the 24-pin 22V10 device. In addition, they are ideal for low-frequency or low-duty-cycle environments such as line card and peripheral applications, where low power consumption is a priority. Laptop computers and other battery-operated or backed-up equipment, such as hand-held meters and portable communication units, would benefit from the Zero-Power devices.

The PALCE16V8Z and PALCE22V10Z feature a zero-standby power mode. When none of the inputs switch for an extended period, the device will go into standby mode, shutting down most of its internal circuitry, causing the current consumption to drop to almost zero (15 µA). The outputs will maintain the states held before the device went into the standby mode. When any input switches, the internal circuitry is fully enabled, and power consumption returns to normal.

Since all of the features which cause the device to be a Zero-Power PLD are internal, the 16V8Z and the 22V10Z PAL devices are pin-for-pin and JEDEC-file compatible with existing devices of the same families.

HINTS ON MINIMIZING POWER CONSUMPTION

The quintessential feature of the ZPAL device's current reducing operation is the "sleep mode." When the device is inactive for a period of time, certain portions of the PLD can be disabled or "put to sleep" by the presence of input transition detection circuitry. Any switching delays of about 50 nanoseconds or more, for the entire device, will place the PLD in sleep mode. This means that none of the inputs, including the clock, can be switching in order to utilize the significant power saving features. Therefore, during the design phase, special attention must be given to *every* signal that is being transferred to the device, so that the sleep mode feature may be engaged as much as possible. Refer to Figure 1 for ZPAL device features.

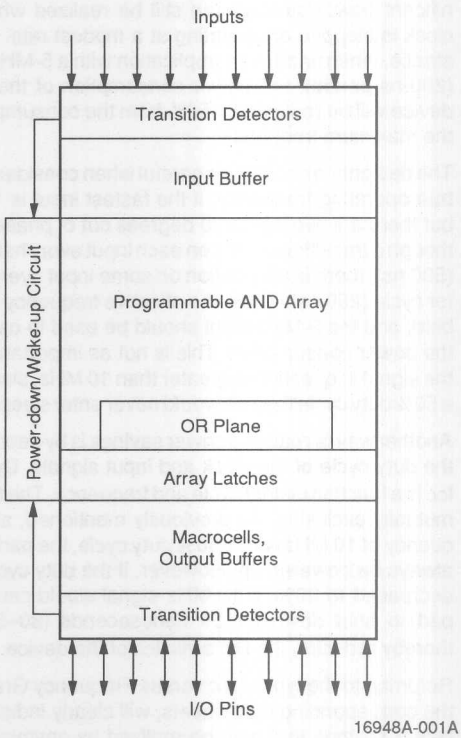


Figure 1. ZPAL Device Features

Publication# 16948 Rev. A Amendment /0
Issue Date: June 1992

As sleep mode is asserted, all outputs will latch to the state they were in when the last input transition occurred. This state will be held as long as the device is asleep.

When an input does experience a transition, the device will "wake up." The wake-up delay associated with the initial transition is included in the determined propagation delay of the device, which is 25 nanoseconds. Therefore, there are no extra system delays to consider when the device utilizes the standby feature, since it quickly returns to full operation. However, if a designer is more interested in high speed, such as a burst mode application, a typical propagation delay would be closer to 20 nanoseconds while the device is awake.

The inputs and I/O pins are monitored by an input transition detection circuit. Any transition on any pin, including noise spikes, will disengage the sleep mode. Thus, during the design phase, care should be taken to ensure that *all* circuitry associated with the Zero-Power device is as quiet as possible.

Effects of Frequency

The sleep mode benefits are best realized in combinatorial applications since sequential functions will be powered-up with every edge of the clock. However, significant power savings can still be realized when the clock is stopped or operating at a modest rate. For instance, when used in an application with a 5-MHz clock (200-ns period), the power consumption of the ZPAL device will be reduced by 50% from the consumption at the maximum frequency.

The designer must also be careful when considering the true operating frequency. If the fastest input is 1 MHz, but there are two inputs 90 degrees out of phase, even though a transition occurs on each input every half-cycle (500 ns), there is a transition on some input every quarter cycle (250 ns). Thus, the effective frequency is doubled, and the 2-MHz point should be used to calculate the power consumption. This is not as important when the signal in question is greater than 10 MHz, since with a 50% duty cycle the part would never enter sleep mode.

Another way of realizing power savings is by decreasing the duty cycle of the clock and input signals. Dynamic I_{CC} is a function of duty cycle and frequency. The two are mutually exclusive. As previously mentioned, at a frequency of 10 MHz with a 50% duty cycle, the part would always be powered up. However, if the duty cycle was decreased to 20%, a 10-MHz signal would cause the part to shut down for 30 nanoseconds (80–50 ns), thereby reducing the Dynamic I_{CC} of the device.

Referring to the typical Icc versus Frequency Graphs of the corresponding data sheets, will clearly indicate the power savings that may be realized by optimizing the ZPAL device's operating frequency.

Effects of Product Terms

To further reduce power consumption, unused product terms are permanently disabled during programming. Each product term has a Sense Amp Off (SAOFF) bit, which will be programmed when the corresponding product term is unused, thereby shutting off the sense amp to save power. Note that the SAOFF bit is automatically configured and has no effect on the JEDEC file, so the designer does not even have to think about it. A typical power savings of approximately 300 µA per unused product term will be achieved. Thus, a logic design that utilizes a minimum number of product terms will result in the maximum amount of power savings.

Inverting simplified logic by using DeMorgan's theorem and changing the output polarity is one way that a designer may easily reduce product term requirements. For example, in the equation

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Z = X+Y
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the "OR" function denoted by the "+" sign, requires two product terms, one for each variable. However, if both sides of the equation are inverted to become

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/Z = /(X+Y)
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using DeMorgan's theorem yields

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/(X+Y) = /X*/Y
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Here the "AND" function denoted by the "*" sign does not use the second product term, because one product term is shared by both variables. The resultant equation is now

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/Z = /X*/Y
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and by switching the output polarity, the logic behaves the same way as it was originally intended as well as reducing a product term requirement.

The choice of output polarity itself does not save power, but if chosen wisely, it may help to reduce product term usage. It should also be noted, however, that switching output polarity will also invert the Synchronous Preset (SP) and Asynchronous Reset (AR) functions at the output of the register of a 22V10.

I/O Characteristics

The output stage of the Zero-Power PAL devices consist of a P-channel pull-up transistor and an N-channel pull-down transistor, a true CMOS output with rail-to-rail switching. A P-channel pull-up is better for low-power applications than an N-channel transistor, since P-channel outputs can be driven up to the V_{CC} level. This ensures that the following input buffer draws no current. The same amount of current is available for both high and low outputs with a P-channel pull-up, unlike the unequal, although slightly faster N-channel transistor used in other PLD products.

These devices are capable of driving and being driven by either TTL or CMOS devices. They are compatible with both HC and HCT standard specifications as illustrated in Table 1.

Table 1

Parameter	HC	HCT	ZPAL
V_{IH}	3.15 V	2.0 V	2.0 V
V_{IL}	0.9 V	0.8 V	0.9 V
V_{OL} @ 6 mA	0.33 V	0.33 V	0.33 V
V_{OL} @ 20 µA	0.1 V	0.1 V	0.1 V
V_{OH} @ 6 mA	3.84 V	3.84 V	3.84 V
V_{OH} @ 20 µA	V_{CC} –0.1 V	V_{CC} –0.1 V	V_{CC} –0.1 V

One minor disadvantage of true CMOS outputs is the intrinsic SCR circuit that is developed in the CMOS structure and cannot be eliminated. The SCR has been made as difficult as possible to turn on by using guard rings and carefully laying out all input and output circuits. An excess current of 100 mA would be required on an individual pin to induce "latch-up". However, there is a potential to latch-up a ZPAL device through hot-socket insertion. If there is a possibility of the device or board being instantly powered-up, design care must be taken.

Effects of Reducing I/O Switching

Since each input will draw up to a maximum of 5 mA each time it switches, additional power savings are possible by reducing the number of inputs used. A CMOS transistor pair only draws current when it is switching or floating in an intermediate region, so unused inputs should be externally tied either HIGH or LOW. The number of outputs switching will also affect the amount of current consumption. Therefore, minimizing output switching will also help to reduce the amount of current required.

The potential for ground bounce problems will also be reduced by limiting the number of outputs switching. Built-in slew-rate-limiting circuits will help to slow down the fast CMOS falling edges that contribute to ground bounce. A fall rate of 1.25 V/ns is typical of the faster N-channel pull-down transistor, while a slower rise rate of 1 V/ns can be expected from the P-channel pull-up. If most of the outputs are required to switch simultaneously, it is important to ensure that the ground path on the circuit board has low inductance, and to reduce the loading on the outputs. The lower-lead-inductance PLCC package will also reduce the possibility of ground bounce since the bonding wires are 1/4 the length of a DIP's bond wires.

Effects of Loading

Power dissipation of the outputs is greatly affected by the load. To minimize power dissipation, ZPAL device loads should have no DC components. If termination is required, an AC terminator like the one in Figure 2 should be used to eliminate DC power drain.

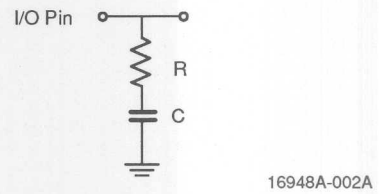

Figure 2. Typical AC Terminator

The capacitance should generally be kept as low as possible since the output stage will go through a process of constantly charging and discharging the capacitor. The formula for current consumption due to loading is

$$i = C_L V s f o$$

where i is the current, C_L is the capacitive load, Vs is the voltage swing, and fo is the frequency at which the output is switching. Therefore, current is consumed every high transition since the capacitor has to recharge.

SUMMARY

ZPAL devices provide zero-standby power and high speed for a variety of applications. Zero-Power CMOS devices can significantly reduce system power consumption by replacing equivalent CMOS and TTL devices. Since all of the features which cause the device to be a Zero-Power PLD are internal, the 16V8Z and the 22V10Z PAL devices may be used in any application where a standard 22V10 or 16V8 device would be used. With a little extra attention given to the particular design involving a Zero-Power PAL device, a designer can realize significant system power savings.

ZPAL™ Devices